



IRAF

February 19, 2009

TO: Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Attn: Art Unit 2891 - Examiner David A Zarneke

FROM: Stephen B. Ackerman, Reg. No. 37,761
28 Davis Avenue
Poughkeepsie, N.Y. 12603

SUBJECT: Serial #: 09/837,007
File Date: April 18, 2001
Inventor: M.S. Lin, et al.
Examiner: David A. Zarneke
Art Unit: 2891
Title: A Structure and Manufacturing Method of a Chip Scale Package

RESPONSE TO FINAL OFFICE ACTION

Dear Sir:

The Final Office Action mailed Dec, 19, 2008 has been carefully considered. In response thereto, please consider the following remarks concerning the above-identified application for patent.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on Feb. 19, 2009.

Stephen B. Ackerman, Reg # 37,761

Signature

Date February 19, 2009